Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A multiplexer comprising:

a first input;

a first differential amplifier of a first channel, the first differential amplifier including a first differential pair of transistors ~~of a first channel~~ coupled to the first input;

a second input;

a second differential amplifier of a second channel, the second differential amplifier including a second differential pair of transistors ~~of a second channel~~ coupled to the second input; ~~and~~

an output;

a first plurality of selection transistors coupled between the first differential pair of transistors and the output; and

a second plurality of selection transistors coupled between the second differential pair of transistors and the output,

~~coupled to the first and second channels,~~ wherein the first ~~and second channels can be~~ channel is selected as active or inactive by the first plurality of selection transistors and the second channel is selected as active or inactive by the second plurality of selection transistors~~, and wherein a collector-base coupling capacitance of the differential pair of the active channel is~~

~~coupled directly to the output, and a collector-base coupling capacitance of the differential pair of the inactive channel is not coupled directly to the output~~.

2. (canceled).

3. (canceled).

4. (currently amended) The multiplexer of claim 1 which includes a ~~non-inverted~~ first select input for activating the first channel and inactivating the second channel and ~~an inverted~~ a second select input for inactivating the first channel and activating the second channel.

5. (currently amended) The multiplexer of claim ~~3~~ 1 wherein when the first channel is inactive or when the first channel is active, a subset of the first plurality of selection transistors ~~are~~ is turned off, and a subset of the first plurality of selection transistors is turned on ~~when the first channel is inactive~~.

6. (currently amended) The multiplexer of claim ~~5~~ 1 wherein when the second channel is inactive or when the second channel is active, a subset of the second plurality of selection transistors ~~are~~ is turned off, and a subset of the second plurality of selection transistors is turned on ~~when the second channel is inactive~~.

7. (previously presented) The multiplexer of claim 1 wherein when the first channel is selected to be active, the second channel is selected to be inactive, and when the second channel is selected to be active, the first channel is selected to be inactive.

8. (currently amended) The multiplexer of claim ~~3~~ 1 which further includes a ~~non-inverted~~ first select input for activating the first channel and inactivating the second channel using ~~at least one~~ a first subset of the first plurality of selection transistors and a first subset of the second plurality of selection transistors, and ~~an inverted~~ a second select input for inactivating the first channel and activating the second channel using ~~at least one~~ a second subset of the second plurality of selection transistors and a second subset of the first plurality of selection transistors.

9. (currently amended) A multiplexer comprising:

a first input;

a first channel including a first input differential amplifier coupled to the first input, and a first plurality of selection transistors coupled to the first input differential amplifier;

a second input;

a second channel including a second input differential amplifier coupled to the second input, and a second plurality of selection transistors coupled to the second input differential amplifier; and

an output coupled to the first and second plurality of selection transistors, wherein [a] selection ~~input~~ inputs provided to the first and second plurality of selection transistors connects either the first channel or the second channel as active for output and the other one of the first channel or second channel as inactive for output~~, such that a collector-base coupling capacitance of~~

~~the input differential amplifier for the active channel is coupled directly to the output, and a collector-base coupling capacitance of the input differential amplifier for the inactive channel is not coupled directly to the output~~.

10. (currently amended) The multiplexer of claim [7] 9 wherein the selection ~~input includes~~ inputs include a ~~non-inverted~~ first select input for activating the first channel and inactivating the second channel, and ~~an inverted~~ second select input for inactivating the first channel and activating the second channel.

11. (currently amended) The multiplexer of claim 10 wherein ~~at least one~~ a first subset of the first plurality of selection transistors is turned off and a second subset of the first plurality of selection transistors is turned on when the first channel is inactive, and wherein ~~at least one~~ a first subset of the second plurality of selection transistors ~~are~~ is turned off and a second subset of the second plurality of transistors is turned on when the second channel is inactive.

12. (currently amended) The multiplexer of claim 11 ~~wherein at least one of the first plurality of transistors is coupled to the collectors of transistors of the first differential amplifier, and at least one of the second plurality of transistors is coupled to the collectors of transistors of the second differential amplifier,~~ wherein the ~~at least one~~ first subset of the first plurality of selection transistors ~~coupled to the collectors of the transistors of the first differential amplifier are~~ is directly coupled to the output, and wherein the ~~at least one~~ second subset of the second plurality of selection transistors ~~coupled to the collectors of the transistors of the second differential amplifier are~~ is not

directly coupled to the output~~, such that the coupling capacitance of the second different amplifier is not directly coupled to the output when the second channel is inactive~~.

13. (currently amended) The multiplexer of claim 12 wherein ~~the at least one~~ the second subset of the second plurality of selection transistors ~~coupled to the collectors of the transistors of the second differential amplifier are~~ is coupled to a positive voltage source ~~Vcc~~.

14. (currently amended) The multiplexer of claim 12 ~~wherein at least one of the second plurality of transistors is coupled to the collectors of transistors of the second differential amplifier, and at least one of the first plurality of transistors is coupled to the collectors of transistors of the first differential amplifier,~~ wherein the ~~at least one~~ first subset of the second plurality of selection transistors ~~coupled to the collectors of the transistors of the second differential amplifier are~~ is directly coupled to the output, and wherein the ~~at least one~~ second subset of the first plurality of selection transistors ~~coupled to the collectors of the transistors of the first differential amplifier are~~ is not directly coupled to the output~~, such that the coupling capacitance of the first differential amplifier is not directly coupled to the output when the first channel is inactive~~.

15. (currently amended) The multiplexer of claim 14 wherein the ~~at least one~~ second subset of the first plurality of selection transistors ~~coupled to the collectors of the transistors of the first differential amplifier are~~ is coupled to a positive voltage source ~~Vcc~~.

16. (new) The multiplexer of claim 4 wherein the first select input is inverted relative to the second select input.

17. (new) The multiplexer of claim 9 wherein the selection inputs include a first selection input provided to particular ones of the first plurality of selection transistors and to particular ones of the second plurality of selection transistors, and a second selection input provided to other ones of the first plurality of selection transistors and other ones of the second plurality of selection transistors.

18. (new) The multiplexer of claim 17 wherein the first selection input is inverted relative to the second selection input.

19. (new) A method for multiplexing input signals, the method comprising:

providing a differential amplifier coupled to each of a plurality of input signals, and providing a plurality of selection transistors coupled between each of the differential amplifiers and an output to isolate the collector-base capacitance of the differential amplifiers from the output; and

using the selection transistors to select at least one of the input signals and differential amplifiers as active for output, and to select at least one of the input signals and differential amplifiers as inactive for output.

20. (new) The method of claim 19 wherein the using of the selection transistors includes providing a first selection signal to a plurality of the selection transistors coupled to each of the differential amplifiers, and providing a second selection signal, inverted relative to the first selection signal, to a different plurality of the selection transistors coupled to each of the differential amplifiers.